forming at least one recess extending from a second surface of the substrate, opposite the first surface, into interior portions of the semiconductor substrate; and

forming at least one resistivity-lowering body in the least one recess of the semiconductor substrate, the at least one resistivity-lowering body comprising a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.

53. A method according to Claim 52 further comprising forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one resistivity-lowering body.

54. A method according to Claim 52 wherein forming the at least one resistivity-lowering body comprises filling an associated recess.

55. A method according to Claim 52 further comprising forming a barrier layer lining the at least one recess.

56. A method according to Claim 52 wherein forming the at least one resistivity-lowering body comprises forming same using an electrical conductor having an electrical resistivity less than about $10^{-4}$ $\Omega$•cm.

57. A method according to Claim 52 wherein forming the at least one recess and associated resistivity-lowering

body comprises forming same to define a proportion of the semiconductor substrate area adjacent the at least one device active region greater than about 0.4 percent.

58. A method according to Claim 52 wherein forming the at least one recess and associated resistivity-lowering body comprises forming same to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

59. A method according to Claim 52 wherein forming the at least one recess and associated resistivity-lowering body comprises forming an array of recesses and associated resistivity-lowering bodies.

60. A method according to Claim 59 wherein forming the array of recesses and associated resistivity-lowering bodies comprises forming same to be arranged in a grid pattern.

61. A method according to Claim 60 wherein forming the grid pattern comprises cutting trenches in the second surface of the semiconductor substrate.

62. A method according to Claim 52 wherein forming the at least one device active region comprises forming at least one device active region for a metal-oxide semiconductor field-effect transistor (MOSFET).

63. A method according to Claim 52 wherein forming the at least one device active region comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

64. A method according to Claim 52 wherein forming the at least one device active region comprises forming at least one active region of a microprocessor.

65. A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising:

forming at least one device active region in the semiconductor substrate adjacent a first surface thereof; and

forming at least one resistivity-lowering body extending from a second surface of the substrate, opposite the first surface, into interior portions of the semiconductor substrate, the at least one resistivity-lowering body comprising a material different than the semiconductor substrate and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate

66. A method according to Claim 65 further comprising forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to the at least one resistivity-lowering body.

67. A method according to Claim 65 wherein forming the at least one resistivity-lowering body comprises forming

same using an electrical conductor having an electrical resistivity less than about $10^{-4}$ Ω•cm.

68. A method according to Claim 65 wherein forming the at least one resistivity-lowering body comprises forming same to define a proportion of the semiconductor substrate area adjacent the at least one device active region greater than about 0.4 percent.

69. A method according to Claim 65 wherein forming the at least one resistivity-lowering body comprises forming same to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

70. A method according to Claim 65 wherein forming the at least one resistivity-lowering body comprises forming an array of resistivity-lowering bodies.

71. A method according to Claim 70 wherein forming the array of resistivity-lowering bodies comprises forming same to be arranged in a grid pattern.

72. A method according to Claim 71 wherein forming the grid pattern comprises cutting trenches in the second surface of the semiconductor substrate.

73. A method according to Claim 65 wherein forming the at least one device active region comprises forming at